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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,776	09/22/2000	Takashi Yoshikawa	05225.0168	8165

22852 7590 11/05/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
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EXAMINER	
ROCHE, TRENTON J	

ART UNIT	PAPER NUMBER
2124	4

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,776	YOSHIKAWA, TAKASHI	
	Examiner	Art Unit	
	Trent J Roche	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-24 have been examined.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/667,776, filed on 09/22/2000.

Drawings

3. The drawings in this application are objected to by the Draftsperson as informal. Any drawing corrections requested, but not made in the prior application should be repeated in this application if such changes are still desired. If the drawings were changed and approved during the prosecution of the prior application, a petition may be filed under 37 CFR 1.182 requesting the transfer of such drawings, provided the parent application has been abandoned. However, a copy of the drawings as originally filed must be included in the 37 CFR 1.60 application papers to indicate the original content. For more information, note form PTO-948 (Notice of Draftsperson's Patent Drawing Review)

4. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

Replacement Drawing Sheets

Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be

presented either in the drawing amendments, or remarks, section of the amendment. Any replacement drawing sheet must be identified in the top margin as "Replacement Sheet" and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. The figure or figure number of the amended drawing(s) must not be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin.

Annotated Drawing Sheets

A marked-up copy of any amended drawing figure, including annotations indicating the changes made, may be submitted or required by the examiner. The annotated drawing sheets must be clearly labeled as "Annotated Marked-up Drawings" and accompany the replacement sheets.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.85(a). Failure to take corrective action within the set period will result in ABANDONMENT of the application.

If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings MUST be filed within the THREE MONTH shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability.

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the application exceeds the maximum 150 word limit.

6. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: "As for at least two task windows continually located in the program..." on page 16 and "consists of a plurality of cues. Each queue in the execution buffer..." on page 17 of the specification.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,511,172 to Kimura et al.

Regarding claim 1:

Kimura et al teach:

- a central processing apparatus for assigning instructions of a program to a plurality of buffers each connected to one of a plurality of execution units, the plurality of execution

units each executing the instructions by accessing a memory and a global register (Note Fig. 1, elements 1, 3, 4, 6, 8-11 and 19 and the corresponding sections of the disclosure)

- a plurality of instruction sequences including a data dependency (Note Figures 5 and 10 and the corresponding section of the disclosure)
- a task window number generator configured to assign a task window number to the instruction sequences (Note Fig. 6 and the corresponding section of the disclosure. A number generator must inherently be present such that the proceeding and succeeding instruction sequences are arranged in the correct order.)
- an assignment unit configured to assign the instructions to the plurality of buffers ("The instruction fetch unit prefetches instructions from the memory...and selectively writes them into the instruction fetch buffers..." in col. 7 lines 10-13)
- a register update unit configured to update data in the register number ("The execution order management buffer stores the results of the speculative execution accompanied with their register numbers and modes." in col. 7 lines 52-54)
- a memory update unit configured to update data in the memory address accessed by a particular instruction sequence ("a fetch controlling device for...incrementing its address every time an instruction is fetched from the memory..." in col. 3 lines 6-9)

as claimed.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Kimura et al teach each instruction sequence including non-speculative instructions as claimed (Note col. 12 lines 10-50, wherein the execution of the instruction sequences is described.

Regarding claim 3:

The rejection of claim 2 is incorporated, and further, Kimura et al teach instructions in the program being aligned in correspondence with each of the plurality of execution units to execute the each instruction in parallel as claimed ("a plurality of executing units for processing in parallel a plurality of instructions..." in col. 1 lines 60-62)

Regarding claim 4:

The rejection of claim 3 is incorporated, and further, Kimura et al teach a condition instruction, the task numbers to be accepted if the condition is not satisfied as claimed (Note col. 4 line 65 to col. 5 line 8)

Regarding claim 5:

The rejection of claim 4 is incorporated, and further, Kimura et al teach a commit instruction representing a branch condition instruction as claimed ("three types of Branch with Condition Code Instructions..." in col. 6 lines 49-50)

Regarding claim 6:

The rejection of claim 3 is incorporated, and further, Kimura et al teach a loop condition instruction as claimed (Note Fig. 4 and the corresponding section of the disclosure.)

Regarding claim 7:

The rejection of claim 3 is incorporated, and further, Kimura et al teach a global register comprising a plurality of register numbers as claimed (Note Fig. 1, item 20 and the corresponding section of the disclosure, and further, col. 4 lines 5-11)

Regarding claim 8:

The rejection of claim 7 is incorporated, and further, Kimura et al teach an instruction decoder configured to decode a plurality of the instructions in order as claimed (Note Fig. 3 and the corresponding section of the disclosure.)

Regarding claim 9:

The rejection of claim 8 is incorporated, and further, Kimura et al teach an instruction decoder decoding the instruction including the flag, and setting the register number in the global register represented by the flag as claimed ("The scoreboard managing circuit checks which registers are in operation by referring to the scoreboard, and set the flags in the scoreboard based on the decoding of the decoders..." in col. 10 lines 19-22)

Regarding claim 10:

The rejection of claim 3 is incorporated, and further Kimura et al teach a plurality of queues, each of the plurality of queues exclusively storing the instructions by first in first out as claimed ("The instruction fetch buffers...send the prefetched instructions to the instruction fetch buffer using FIFO(First-In-First-Out) memories." in col. 7 lines 25-27)

Regarding claim 11:

The rejection of claim 10 is incorporated, and further Kimura et al teach assigning the instruction to the queue in the execution buffer as claimed ("The execution order management buffer stores the results of the speculative execution accompanies with their register numbers and modes." in col. 7 lines 52-54.)

Regarding claim 12:

The rejection of claim 1 is incorporated, and further, Kimura et al teach incrementing the task window n umber by one when the commit instruction is detected as claimed (Note col. 2 line 66 to col. 3 line 17.)

Regarding claim 13:

The rejection of claim 9 is incorporated, and further, Kimura et al teach a plurality of local registers respectively connected to each of the plurality of execution units as claimed (Note Fig. 10, which displays a list of Register numbers an instruction is written to, and the execution result of the instruction.)

Regarding claim 14:

The rejection of claim 13 is incorporated, and further, Kimura et al teach a register update unit updating data in the register number of the global register represented by the flag in the particular instruction sequence using the execution result as claimed ("outputs the execution results to the

execution order management circuit, which writes them directly into the register file..." in col. 11 lines 42-44)

Regarding claim 15:

The rejection of claim 13 is incorporated, and further, Kimura et al teach a register update unit which does not update data in the register number of the global register as claimed (Note col. 10 lines 33-43. The instruction issuing circuit rejects instructions that do not meet the criteria, which in turn does not update the data in the register.)

Regarding claim 16:

The rejection of claim 1 is incorporated, and further, Kimura et al teach a memory update unit which temporarily preserves the execution result of a store instruction as claimed ("the execution result managing means includes temporary for storing means storing a set of the execution results of the executing units..." in col. 22 lines 58-61)

Regarding claim 17:

The rejection of claim 16 is incorporated, and further, Kimura et al teach a memory update unit which updates data in the address of the memory represented by the store instruction as claimed ("the temporary storing means stores register numbers of the execution results when the results are to be stored into registers, and stores memory addresses thereof when they are to be stored in the memory." in col. 22 lines 63-67)

Regarding claim 18:

The rejection of claim 16 is incorporated, and further, Kimura et al teach a memory update unit which does not update data in the address of the memory as claimed (Note that col. 22 lines 63-67 disclose storing into memory when the results only when the results are to be stored, consequently, the system will inherently not update data in the address of the memory when an instruction is not meant to be stored.)

Regarding claim 19:

The rejection of claim 16 is incorporated, and further, Kimura et al teach a load buffer which temporarily preserves a load instruction from memory as claimed (Note Fig. 1 elements 3 and 4 and the corresponding sections of the disclosure.)

Regarding claim 20:

The rejection of claim 19 is incorporated, and further, Kimura et al teach an execution unit which executes the load instruction in a particular instruction, and decides whether the load instruction depends on the execution result of the store instruction as claimed ("The processor may further comprise a data-dependence detecting device for detecting data-dependence among a plurality of the decoded instructions by referring to a plurality of decoding results..." in col. 3 lines 45-48)

Regarding claim 21:

The rejection of claim 20 is incorporated, and further, Kimura et al teach a load buffer which loads the execution result of the store instruction as claimed ("Instruction N-2 is not issued until Instruction N-3 has been completed due to data-dependence." in col. 11, lines 35-37. Further, all instruction are stored in an instruction fetch buffer.)

Regarding claim 22:

The rejection of claim 21 is incorporated, and further, Kimura et al teach a load buffer loading data stored in the address of the memory as claimed ("The instruction issuance allowing device may identify instructions with issuable ones by confirming that the decoding results of the plurality of the decoding device have no data-dependence among each other from the detecting result of the data-dependence detecting device..." in col. 3 lines 61-65)

Regarding claim 23:

Claim 23 is directed to a compile method for generating a program to perform the actions as described in claim 1, and are rejected for the reasons set forth in connection with claim 1. Further, while Kimura et al do not disclose a compile method directly, there is inherently a compilation process used to generate a program to control the distribution of parallel instructions in the system of Kimura et al.

Regarding claim 24:

Claim 24 is directed to a computer readable memory containing computer readable instructions in a computer for performing the actions as described in claim 1, and are rejected for the reasons set forth in connection with claim 1.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (703)305-4627. The examiner can normally be reached on Monday-Friday, 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Trent J Roche
Examiner
Art Unit 2124

TJR

Hoanguan Antony Nguyen Ba

ANTONY NGUYEN-BA
PRIMARY EXAMINER